Code No: 154AN

R18

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year II Semester Examinations, August/September - 2021
DIGITAL ELECTRONICS
(Electrical and Electronics Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Write the Properties/Laws of Boolean algebra?
b) A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What is the original 8 bit word if the 12 bit read out is 1010 1001 1101. [8+7]

2.a) Compare different logic families.
b) Realize 2-input NAND gate using CMOS logic. [7+8]

3.a) Find F in POS form for F (A, B, C, D) = Π (1, 3, 7, 11, 15) + d (0, 2, 5).
b) Simplify the function F (A, B, C, D) = Σ (0, 1, 3, 4, 6, 8, 15) using K-Map. [7+8]

4.a) Design a full adder and implement it using multiplexer.
b) Design a 3 to 8 decoder circuit using 2 to 4 decoder circuits. [8+7]

5.a) What is the difference between edge triggering and level triggering? Explain about edge triggered D flip-flop with a neat diagram.
b) Draw the schematic circuit of J-K flip-flop and explain its operation with the help of truth table. [7+8]

6.a) Design a Modulo-7 synchronous counter using J K Flip-Flop. Draw its state diagram and Timing Waveforms.
b) Implement a 3-bit down counter using D flip flop. [8+7]

7.a) Explain the weighted resistor type D/A converter with neat block diagram.
b) A dual slope ADC uses a 16-bit counter and a 4 MHz clock rate. The Maximum input voltage is =10V. The maximum integrator output voltage should be -8V when the counter has cycled through 2n counts. The capacitor used in the integrator is 0.1μF. Find the value of the resistor R of the integrator. If the analog signal is = 4. 129 V, find the corresponding binary number. [8+7]

8.a) What are the draw backs of PLAs? How PLAs are used to implement combinational and sequential logic circuits?
b) Explain the detailed logic configurable Block Architecture of FPGA. [7+8]

---ooOoo---